1. A method to form metal silicide gates in the fabrication of an integrated circuit device, said method comprising:

forming polysilicon lines overlying a substrate wherein said polysilicon lines have dielectric sidewalls;

forming a first isolation layer overlying said substrate and said dielectric sidewalls wherein said first isolation layer does not overlie the top surface of said polysilicon lines;

partially etching down said polysilicon lines such that said top surfaces of said polysilicon lines are below the top surface of said dielectric sidewalls;

thereafter depositing a metal layer overlying said polysilicon lines;

thermally annealing to completely convert said polysilicon lines to metal silicide gates; and

removing unreacted said metal layer to complete said device.

2. The method according to Claim 1 wherein said step of forming polysilicon lines further comprises:

forming a dielectric layer overlying said substrate;

depositing said polysilicon layer overlying said dielectric layer;

depositing a hard mask layer overlying said polysilicon layer;

patterning said hard mask layer; and

patterning said polysilicon layer to form said polysilicon lines as defined by said hard mask layer pattern.

3. The method according to Claim 2 wherein said hard mask layer is removed prior to said step of partially etching down said polysilicon lines.

4. The method according to Claim 1 wherein said step of forming a first isolation layer further comprises:

depositing an interlevel dielectric layer overlying said substrate and said polysilicon lines; and

planarizing said interlevel dielectric layer.

5. The method according to Claim 1 further comprising implanting ions into said substrate prior to said step of forming a first isolation layer to thereby form first doped regions in said substrate and adjacent to said polysilicon lines.

6. The method according to Claim 1 further comprising:

depositing a spacer layer overlying said substrate and said polysilicon lines;

etching back said spacer layer to from spacers on said sidewalls of said polysilicon lines; and

implanting ions into said substrate to thereby form second doped regions in said substrate and adjacent to said spacers.

7. The method according to Claim 6 wherein said polysilicon lines are covered by a hard mask layer prior to said step of partially etching down said polysilicon lines and further comprising:

depositing a second metal layer overlying said substrate, said spacers, and said hard mask layer prior to said step of partially etching down said polysilicon lines;

thermally annealing to convert a part of said substrate in said second doped regions to metal silicide; and

removing unreacted said second metal layer.

8. The method according to Claim 6 wherein said spacers have a width of between about 200 Å and about 1000 Å.

9. The method according to Claim 1 wherein said dielectric layer for a first group of said metal silicide gates is a first thickness, wherein said dielectric layer for a second part of said metal silicide gates is a second thickness, and wherein said first and second thicknesses are not equal.

10. The method according to Claim 1 wherein said step of partially etching down said polysilicon lines results in a thickness of said polysilicon lines of between about 100 Å and about 500 Å.

11. The method according to Claim 1 wherein said metal silicide gates have a thickness of between about 180 Å and about 900 Å.

12. A method to form metal silicide gates in the fabrication of an integrated circuit device, said method comprising:

forming said dielectric layer overlying a substrate;

depositing said polysilicon layer overlying said dielectric layer;

depositing a hard mask layer overlying said polysilicon layer;

patterning said hard mask layer;

patterning said polysilicon layer to form polysilicon lines as defined by said hard mask layer pattern;

forming a first isolation layer overlying said substrate and said polysilicon lines wherein said first isolation layer does not overlie said hard mask layer;

removing said hard mask layer;

thereafter partially etching down said polysilicon lines such that the top surfaces of said polysilicon lines are below the top surface of said first isolation layer;

thereafter depositing a metal layer overlying said polysilicon lines;

thermally annealing to completely convert said polysilicon lines to metal silicide gates; and

removing unreacted said metal layer to complete said device.

13. The method according to Claim 12 wherein said step of forming a first isolation layer further comprises:

depositing an interlevel dielectric layer overlying said substrate and said polysilicon lines; and

planarizing said interlevel dielectric layer.

14. The method according to Claim 12 wherein said step of forming a first isolation layer further comprises:

depositing a spacer layer overlying said substrate and said polysilicon lines; and

etching back said spacer layer to from spacers on said sidewalls of said polysilicon lines.

15. The method according to Claim 12 further comprising implanting ions into said substrate prior to said step of forming a first isolation layer to thereby form first doped regions in said substrate and adjacent to said polysilicon lines.

16. The method according to Claim 15 wherein said step of forming a first isolation layer further comprises:

depositing a spacer layer overlying said substrate and said polysilicon lines;

etching back said spacer layer to from spacers on said sidewalls of said polysilicon lines; and

implanting ions into said substrate to thereby form second doped regions in said substrate and adjacent to said spacers.

17. The method according to Claim 16 further comprising:

depositing a second metal layer overlying said substrate, said spacers, and said hard mask layer;

thermally annealing to convert a part of said substrate in said second doped regions to metal silicide; and

removing unreacted said second metal layer.

18. The method according to Claim 12 wherein said dielectric layer for a first group of said metal silicide gates is a first thickness, wherein said dielectric layer for a second part of said metal silicide gates is a second thickness, and wherein said first and second thicknesses are not equal.

19. The method according to Claim 12 wherein said step of partially etching down said polysilicon lines results in a thickness of said polysilicon lines of between about 100 Å and about 500 Å.

20. The method according to Claim 12 wherein said metal silicide gates have a thickness of between about 180 Å and about 900 Å.

21. A metal silicide gate MOS device, said device comprising:

a metal silicide gate overlying a substrate with a dielectric layer therebetween; and

spacers on the sidewalls of said metal silicide gate wherein said spacers are substantially taller than said metal silicide gate.

22. The device according to Claim 21 further comprising first doped regions in said substrate wherein said first doped regions are adjacent to edges of said metal silicide gate.

23. The device according to Claim 22 further comprising second doped regions in said substrate wherein said second doped regions are adjacent to said spacers.

24. The device according to Claim 21 further comprising metal silicide regions in said substrate wherein said metal silicide regions are adjacent to said spacers.

25. The device according to Claim 21 wherein said metal silicide gate has a thickness of between about 100 Å and about 900 Å.